PATENT
Atty. Docket No.: ALSC-00300

#5/Reply for Recons. Shrivastava 2/17/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Shrivastava

Serial No. 09/315,599

Filed: 05/20/99

For: **METHOD AND APPARATUS FOR INTEGRATING FLASH EEPROM AND SRAM CELLS ON A COMMON SUBSTRATE**

Group Art Unit: 2814
Examiner: Ha, N.

AMENDMENT AND RESPONSE TO OFFICE ACTION MAILED ON Nov. 8, 2000

260 Sheridan Ave., Suite 420
Palo Alto, CA 94306
(650) 833-0160

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

REMARKS

Applicants respectfully request further examination and reconsideration in view of the comments set forth fully below. Within the Office Action, all of the Claims 1-10 were rejected. Claims 1-10 still remain pending.

Rejections Under 35 U.S.C. § 103

Claims 1-3, 5, and 7-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,679,599 to Mehta (hereinafter "Mehta") in view of U.S. Patent No. 6,133,640 to Leedy (hereinafter "Leedy"). Mehta teaches a device and method for isolating regions of the circuit device in a semiconductor substrate. The method comprises the

following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. [Mehta, Abstract and col. 4, line 46- col. 6, line 49] Mehta does not teach a separation technique for growing flash EPROM and SRAM on a common substrate.

Leedy teaches a three dimensional structure memory or a stacked memory device using fine-grain high density inter-layer vertical bus connections. Leedy teaches a physical separation of the memory circuits and the control logic circuit onto different layers such that each layer may be separately optimized. [Leedy, Abstract] The fine-grain inter-layer vertical interconnects electrically interconnect the stack of memory circuits. [Leedy, col. 4, lines 1-8] Leedy teaches that the three dimensional structure memory devices are stacked on one another, or on a conventional IC using the fine-grain interconnect technique. [Leedy, col. 4, lines 35-40] Each memory array layer includes a memory array circuit composed of array blocks and each block is composed of memory cells. [Leedy, col. 4, lines 53-58 and Figs. 2a, 2b.] The controller circuit is located on a different layer and is described in detail by Leedy. [Leedy, col. 6, line 52-col. 7, line 8 and Fig. 2c.]

Leedy does not teach the implementation of both SRAM and flash EPROM on the same layer. In fact, Leedy only suggests the implementation of either SRAM or flash EPROM but not both. Leedy teaches, "each block is composed of memory cells (in much the same manner as the cell array of a DRAM **or** EEPROM circuit," [Leedy, col. 4, lines 56-57] Furthermore, within the Office Action it is stated that Leedy discloses the structure of SRAM and EEPROM in a common substrate. The applicant respectfully disagrees with this interpretation of Leedy. In col. 1, lines 43-50, Leedy states:

> Integrated circuit memory such as DRAM, SRAM, flash EPROM, EEPROM, Ferroelectric, GMR (Giant MagnetoResistance), etc. have the common architectural or structural characteristic of being monolithic with the control circuitry integrated on the same die with the memory array circuitry. This established (standard or conventional) architecture or circuit layout structure creates a design trade-off constraint between control circuitry and memory array circuitry for large memory circuits.

The above quotation means that the memory array circuitry and the control circuitry are integrated in the same die for each type of IC circuit memory such as DRAM, SRAM, flash EPROM, EEPROM, etc. When the memory array on the die becomes denser, the control

circuitry also becomes denser. [Leedy, col. 1, lines 53-60] That is why Leedy states that this kind of conventional and standard package has serious problems. The above quotation from Leedy does not suggest that SRAM and flash EPROM can be integrated on a common substrate.

In contrast to the teachings of Mehta, Leedy and their combination, the present invention teaches a system for and a method of integrating SRAM cells and flash EPROM cells onto a single silicon substrate. The common substrate includes an area where a local oxidation of silicon (LOCOS) isolation technique is implemented and in another area on the same silicon substrate where a shallow trench isolation technique (STI) is implemented. As described above, neither Mehta, Leedy nor their combination teach integrating both SRAM cells and flash EPROM cells onto a common substrate.

The independent Claim 1 is directed to a semiconductor device which comprises a common substrate, an SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. As described above, Mehta, Leedy nor their combination teach nor suggest this. Neither Mehta, Leedy nor their combination teach implementing an SRAM device, isolated by a first isolation technique, on a common substrate with a flash EPROM device, isolated by a second isolation technique. For at least these reasons, the independent Claim 1 is allowable over the teachings of Mehta, Leedy and their combination.

Claims 2 and 3 are both dependent on the independent Claim 1. As discussed above, the independent Claim 1 is allowable over the teachings of Mehta, Leedy and their combination. Accordingly, the dependent Claims 2 and 3 are both also allowable as being dependent on an allowable base claim.

The independent Claim 5 is directed to a system for allowing different types of isolation techniques during fabrication of a semiconductor device. The system of Claim 5 comprises a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing. The system of Claim 5 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device, implemented on the second portion of the substrate. As discussed above, neither Mehta, Leedy nor their combination teach implementing an SRAM device, isolated by a first isolation technique, on a common substrate with a flash EPROM device, isolated by a second isolation technique. For at least these reasons, the independent Claim 5 is allowable over the teachings of Mehta, Leedy and their combination.

Claims 7 and 8 are all dependent on the independent Claim 5. As discussed above, the independent Claim 5 is allowable over the teachings of Mehta, Leedy and their combination.

Accordingly, the dependent Claims 7 and 8 are both also allowable as being dependent on an allowable base claim.

The independent Claim 9 is directed to a semiconductor device comprising a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing. The device of Claim 9 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device implemented on the second portion of the substrate. As discussed above, neither Mehta, Leedy nor their combination teach implementing an SRAM device, isolated by an STI technique, on a common substrate with a flash EPROM device, isolated by a LOCOS isolation technique. For at least these reasons, the independent Claim 9 is allowable over the teachings of Mehta, Leedy and their combination.

Claim 10 is dependent on the independent Claim 9. As discussed above, the independent Claim 9 is allowable over the teachings of Mehta, Leedy and their combination. Accordingly, the dependent Claim 10 is also allowable as being dependent on an allowable base claim.

Within the Office Action, Claims 4, 6 and 10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Mehta and Leedy in view of U.S. Patent No. 6,124,882 to Voois et al. (hereinafter "Voois") Voois teaches a video communicating apparatus and method therefor. Claims 4, 6 and 10 are all dependent on the independent Claims 1, 5 and 9, respectively. As discussed above, the independent Claims 1, 5, and 9 are all allowable over the teachings of Mehta, Leedy and their combination. Accordingly, the dependent Claims 4, 6 and 10 are all allowable as being dependent on an allowable base claim.

For the reasons given above, applicants respectfully submit that the claims are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (650) 833-0160 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: February 8, 2001

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No. 37,902
Attorneys for Applicant(s)

CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

HAVERSTOCK & OWENS LLP

Date: 2/8/01 By: